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LIMITATIONS OF A STATIC VAr COMPENSATOR (SVC) WITH SWITCHED CAPACITOR OPERATING AS AN ACTIVE FILTER

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Abstract: The goal of this paper is to analyze the limitations of a static VAr compensator (SVC) with switched capacitor, when this operate as an active filter.
The limitations considered and studied by simulation are in the zone of ability/inability of the active filter to produce current waveforms and waveforms with the desired di/dt of the desired line current, and from the zone of the operating constraints. The active filter limitations at the desired harmonic frequency *hf* were quantified with the help of two measures: percentage magnitude error and phase error, in the both capacitive and inductive operation modes.

Keywords: Static converter with switched capacitor, Modeling and simulation, Constraints and limitations in active filter operation mode.

1. INTRODUCTION

The power electronics converters from a number of low-power electronic based appliances such as TV sets, personal computers, adjustable speed drivers (heat pumps for space heating and air conditioning, ventilators etc.) HF fluorescent lighting, induction cooking, induction heating, electric welding etc., generate a large amount of harmonic from current in power systems. Voltage distortion or harmonic resulting from current harmonics produced by power electronics equipment has become a serious problem to be solved in many countries.

The basic principles of active filters were proposed in the beginning of the 1970's (Bird, *et al.*, 1969; Sasaki, *et al.*, 1971; Ametani, 1976; Paterson, *et al.*, 1977; Hucker, *et al.*, 1977). The advance of power electronic technology over the last two decades, and because active filters have been studied by many researchers, engineers and Ph.D. students, has been made it possible to put active filters into practical applications for harmonic compensation, flicker compensation and voltage regulation. In present, these above three applications of short shunt filters have been put on a commercial base in Japan, and their rating or capacity has ranged from 50 KVA to 50 MVA (Akagi, 1995).

On the other hand, several Flexible AC Transmission Systems (FACTS) devices are either on the market today (USA, Japan, Europe) or being developed (Gavrilovic, *et al.*, 1983; IEEE Special Stability Controls Working Group, 1994; Rajkumar *et al.*, 1994; Zhao, *et al.*, 1995; Vasconcelos, *et al.*, 1992; Arabi, *et al.*, 1996).

Initially, FACTS devices mainly employed the anti-parallel back-to-back thyristor valve configuration to control/switch RLC/transformer components. Applications of this technology started with the Static VAr Compensators (SVC) in the 1970's (Gavrilovic *et al.*, 1983; IEEE Special Stability Controls Working Group, 1994), and followed by Thyristor-Controlled Series Compensation (TCSC) schemes, in more recent years (Urbanek, *et al.*, 1993; Ionescu, *et al.*, 1998).

Thyristor-Controlled Phase Regulators (TCPR) and Thyristor-Controlled Braking Resistors (TCBR) are expected to follow in the near future, after the paper (Wang, *et al.*, 1994).

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A newer generation of FACTS devices is based on the self-commutated Voltage-Sourced Converted (VSC) using Gate-Turn-Off (GTO) thyristor technology. It includes the Static Condenser (STATCON), Series Power Flow Controller (SPFC), VSC-based Static Phase Shifter (SPS), and Unified Power Flow Controller (UPFC) (Arabi, *et al.*, 1996; Urbanek, *et al.*, 1993; Ionescu, *et al.*, 1998; Wang, *et al.*, 1994; Mohan, *et al.*, 1995).

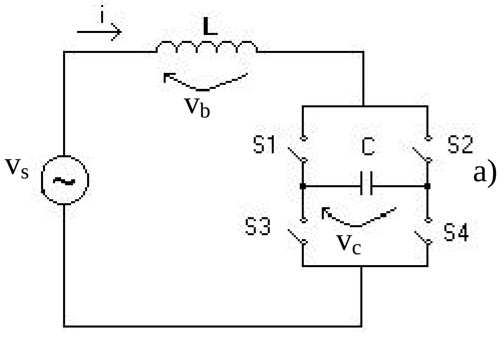
Step-by-step, very probable, the function of active filters will be expanded in future from harmonic compensation, voltage flicker compensation or voltage regulation into power quality improvement for power distribution systems as the capacity of active filters becomes larger. It is possible, perhaps, as the differences between FACTS devices and active filters and/or active power line conditioners to vanished in future, and a new family with a generic name of power quality conditioners will appear.

Among the lots of active filters as configurations (shunt, series, hybrid active and passive, voltage-/current-fed PWM inverter as power circuit, frequency -/or time-domain as control strategies etc.), the circuit analysed here from the point of view of the circuit when operating as an active filter, was firstly mentioned in (Chakravorti, 1992).

Because this circuit is possible to operate not only as a 50 Hz reactive power compensator but and as an active filter, were analysed the limitations and the operating constraints of the circuit, with non-sinusoidal current waveform (Judele, 2001).

2. THE ELEMENTARY SWITCHED CAPACITOR CIRCUIT OF CONVERTER (SCC)

The elementary SCC is shown in Fig. 1. The converter consists in a bridge circuit with a capacitor load C. For the implementation of each bidirectional switch Si, i=1,2,3,4 is possible to be used two back to back transistor-diode modules. Each switch acts like a bidirectional valve, with flexibility in the performance of this circuit and with a relative simple control strategy.



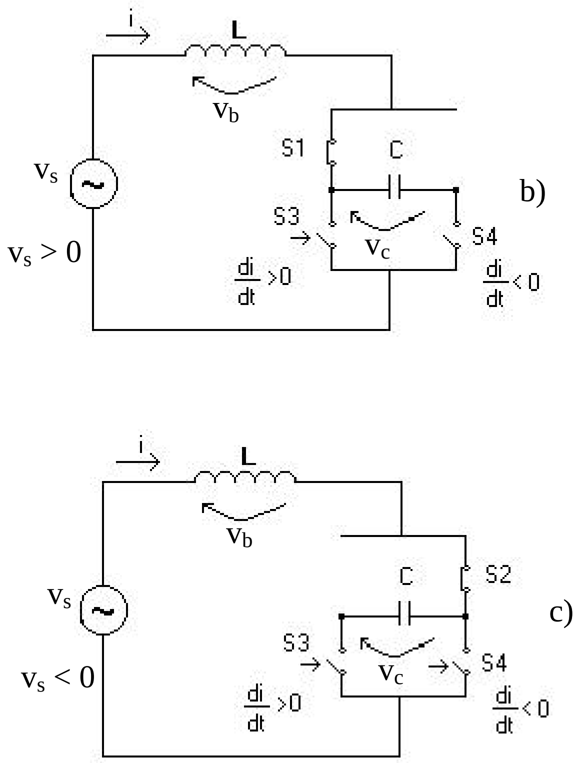


Fig. 1. The basic circuit of the SCC

The source voltage v_s is sinusoidal, the capacitor is precharged with an initial voltage V_0, the coil L has an initial current of I_0, and i is confined within two closely bound limits (a template) which follows the waveforms of $-(i_q+i_h)$, Fig. 2.

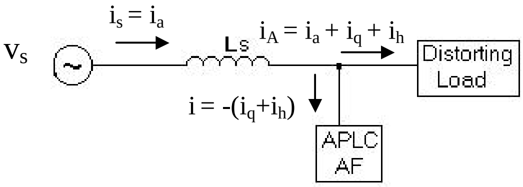


Fig. 2 Basic operating principle of an APLC

The compensating device APLC/AF is meant to draw a current $i = -(i_q + i_h)$, and thus, i_s, the total current drawn from the source by the load and the APLC combination, is only i_a (fundamental active, in phase with the fundamental wave of the source voltage (Judele, 2001)).

The switches are operating in the following sequences: 1) for the time $0<t<T/2$, switch S1 is close and S2 is open; 2) for the time $T/2<t<T$, switch S1 is open and S2 is close; 3) for the time $0<t<t_s$, switch S3 is close and S4 is open, causing di/dt to be positive; 4) for the time $t_s<t<t_i$, switch S3 is open and S4 is clos causing di/dt to be negative.

For the period $0<t<t_s$, keeping switches S1 and S3 closed helps maintain

$$\frac{di}{dt} = \frac{v_s}{L} > 0 \qquad (1)$$

and during $t_s<t<t_i$, keeping switches S1 and S4 closed helps maintain

$$\frac{di}{dt} = \frac{v_S - v_C}{L} < 0\text{, since } v_c>v_s \qquad (2)$$

Thus, at time $t=t_s$, when the current reaches the upper (superior) set limit of the template, switch S3 is opened and switch S4 is closed to obtain a negative di/dt. Again at time $t=t_i$, when the current reaches the lower(inferior) set limit, switch S4 is opened and switch S3 is closed, to obtain a positive di/dt. This process is continued for the entire positive half cycle of v_s to steer the current through the desired waveform. For the negative half cycle of v_s ($T/2<t<T$), switch S1 is kept open and switch S2 is kept closed. Under these circumstances, the effect of closing/opening switches S3 and S4 remains the same. However, this control relies on the fact that $v_c>|v_s|$ at any moment.

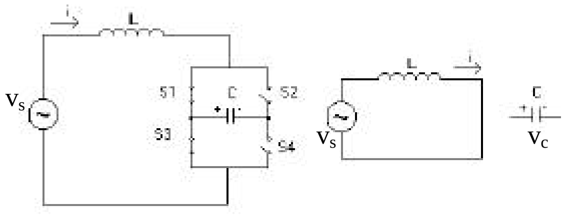
3. MATHEMATICAL MODEL

The converter is operated in such manner that only one of the switches from each of the upper (superior) and the lower (inferior) parts of the converter bridge is conducting at a time. Thus, four different conduction states are identified (see Table 1).

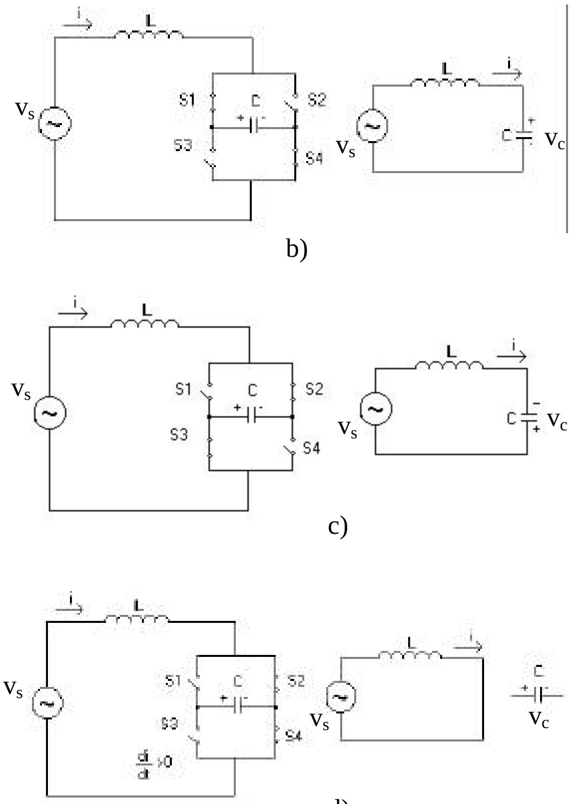
Table 1. Conduction states (modes) of the SCC.

Mode No.	Switches			
	S1	S2	S3	S4
1	closed ($v_s>0$)		conducting when di/dt >0	
2	closed ($v_s>0$)			conducting when di/dt <0
3		Closed ($v_s<0$)	conducting when di/dt <0	
4		Closed ($v_s<0$)		conducting when di/dt <0

The four conduction states (modes) and the equivalent circuits are shown in Fig. 2.



a)



b)

c)

d)

Fig. 3. The four conduction states and the equivalent circuits; a,b,c,d = modes 1,2,3,4 respectively

The conduction transient in each of the conduction modes is computed by modelling the differential equations with the difference equations.

For modes 1 and 4 (n is the discrete time step index):

$$i(n) = \frac{\Delta T}{L} v_S + i(n-1) \qquad (3)$$

$$v_C(n) = v_C(n-1) \qquad (4)$$

For modes 2 and 3:

$$i(n) = \frac{v_S - k \cdot v_C(n-1) + \frac{L}{\Delta T} i(n-1)}{\frac{L}{\Delta T} + \frac{\Delta T}{L}} \qquad (5)$$

$$v_C(n) = \frac{\Delta T}{C} i(n) + v_C(n-1) \qquad (6)$$

where k=1, if $v_s>0$, i.e., mode 2, and k=-1, if $v_s<0$, i.e., mode 3 (Judele, 2001).

To protect the transistors and reduce the switching losses in this circuit used as active filter, turn-off snubbers are used (Fig. 4). As transistors are possible to be used BJTs, IGTBs or MOSFETs; in (Judele, 2001) are used BJTs because were available more information from data sheets about dynamic turn-on and turn-off characteristics, and hence about the dynamics resistors to be modeled in simulation programs.

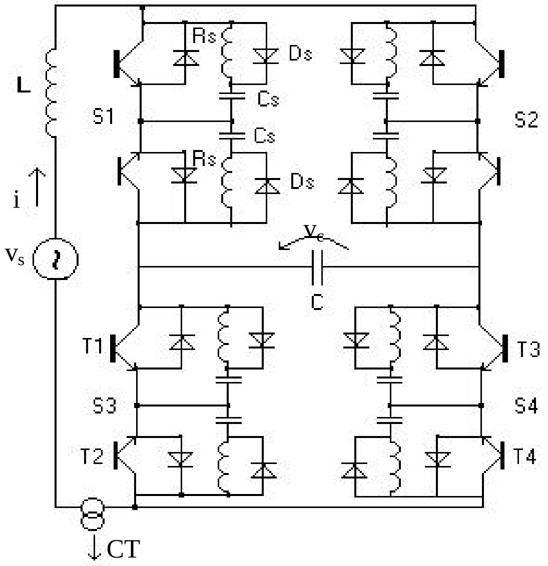


Fig. 4. The converter circuit with switched capacitor and turn-off snubbers for the transistors

4. THE SOURCE-CONVERTER POWER FLOW, WHEN LINE CURRENT CONTAINS USEFUL HARMONICS

In Fig. 1, 3, 4 switches S1 and S2 help direct the flow of energy in each half cycle of v_s whereas the switches S3 and S4 participate in the process of PWM of the switched voltage.

The operation of the circuit as an active filter requires that the line current contain lower order (useful) harmonics besides the fundamental, respectively.

$$i = \pm\sqrt{2}I_1 \cos(\omega t) + \sqrt{2}I_h \sin(h\omega t + \theta_h) \quad (7)$$

For the capacitor voltage, substitution of equations (7) and (8) – voltage source –

$$v_s = \sqrt{2}V \sin \omega t \tag{8}$$

in equation (9), of the balance of power/energy stored in the fields of L and C (Fig.1),

$$p = v_s i = L\frac{di}{dt} + Cv_c\frac{dv_c}{dt} \tag{9}$$

gives (Judele, 2001):

$$\begin{aligned} v_c^2 = V_0^2 &+ \left[-\frac{4I_hV}{C\omega(h^2-1)} \pm \frac{4XI_1I_h}{C\omega}\right]\sin\theta_h - \\ &- \frac{XI_h^2}{C\omega}\cos(2\theta_h) + \frac{XI_1^2 \pm VI_1}{C\omega}(1-\cos(2\omega t)) + \\ &+ \frac{4I_hV}{C\omega(h^2-1)}[\cos(\omega t)\sin(h\omega t+\theta_h) - \\ &- h\sin(\omega t)\cos(h\omega t+\theta_h)] \mp \frac{4XI_1I_h}{C\omega}\cos(\omega t)\cdot\sin(h\omega t+\theta_h) + \\ &+ \frac{XI_h^2}{C\omega}\cos(2h\omega t+2\theta_h). \end{aligned} \tag{10}$$

From the equation (10) we see that the capacitor voltage v_c contains oscillations of 2hf and (h±1)f frequencies. The bridge act receiving input power (active and reactive) at 50 Hz, and supplying output power at dc and harmonic frequency. The power flow can be controlled by adjusting the magnitudes and phase angles of the voltage sources responsible for the oscillations at 2hf and (h±1)f frequencies in the capacitor voltage (10). This is done by the PWM of the switches. The above circuit (Fig. 1,3,4) can perform in three distinctive modes of operation on the desired line current waveform and the type of output load:

i) Converter operation with sinusoidal current waveform, case when the line current is nearly sinusoidal and in quadrature with the voltage. The load is a capacitor or an infinitely large capacitor, case when the normalized resonance frequency (11):

$$\Omega = \frac{1}{\omega\sqrt{LC}} \tag{11}$$

is zero ($\Omega = 0$).

ii) Converter operation with non-sinusoidal current waveform, case when the converter can be called as active filter. Because the main difference between the cases i) and ii) lies in the pattern of the PWM of the switches, the voltage drop across the switches must “cause the generation” of the desired and useful current harmonics (opposed to a sinusoidal line current). In this case the converter provides a controllable and variable amount of reactive power and harmonic current phasors (capacitive or inductive mode).

iii) Converter operation as an active power line conditioner, case when active power is transferred/delivered to/from the output load. The load can be a battery, case when this can be charged or discharged, or, a dissipative/resistive load, case when a storage device as a capacitor or a battery must be connected in parallel to the load, to maintain $v_c = v_s$.

5. LIMITATIONS IN OPERATION OF THE ACTIVE FILTER

5.1 *Limitations and constraints*

The converter operation as active filter is necessary to be studied, to know its capability to compensate line current harmonics. The main limitation of the active filter is its inability to produce current waveforms with the desired di/dt. The waveform of the desired line current is considered to be

$$i = \sqrt{2}I_1\sin(\omega t \pm 90^\circ) + \sqrt{2}I_h\sin(h\omega t + \theta_h) \tag{12}$$

and the RMS value of the line current is

$$i = \sqrt{I_1^2 + I_h^2} \qquad (13)$$

Because the active filter has two conduction modes for each half cycle of the source voltage v_s, the boundary values of the di/dt for the line current depend on the mode of the circuit and are given by:

$$d_i/d_t = v_s/L, \text{ in mode 1} \qquad (14)$$
$$d_i/d_t = (v_s - k \cdot v_c)/L, \text{ in mode 2} \qquad (15)$$

From the equation (14) the di/dt limitation is dependent of v_s and the value of L. The active filter circuit can only cope up with demands of di/dt that are lower than the limit given by equation (14) at any given instant of time. This limitation has a time variation which the same as that v_s (zero at the zero crossings of the v_s, and maximum at the peaks of v_s). From the equation (15), in mode 2, the magnitude of the di/dt limitation is dependent on the difference ($v_s - v_c$), and this limit is time varying as that in mode 1.

But the analytical expression for v_c, when the line current waveform is given by equation (7) is given by the equation (10). Therefore, the time variation of the maximum attainable values of di/dt depends of the v_c, v_s, L, I_h and θ_h. Because of that, as parameters affecting the performance limitations of the active filter were selected the following normalized values:

a) resonance frequency, $\Omega = \frac{1}{\omega\sqrt{LC}}$; b) capacitor initial voltage, $\upsilon = \frac{V_0}{\sqrt{2} \cdot V}$; c) per unit RMS current, $I_{pu} = \frac{I}{V/(L\omega)}$; d) harmonic phase θ_h; e) per unit RMS harmonic current I_h/I.

The converter can operate properly only if the inequality:

$$v_c > |v_s| \qquad (16)$$

is satisfied, inequality which is an important constraint of the active filter operation. Besides, the di/dt limitations in the two conduction modes of the circuit may cause the generation of a line current considerably different than the desired current waveform. Therefore, and the effect of the a) – e) above parameters is analyzed to establish the di/dt limitations.

Thus: $\Omega = f(L, C)$, determines the di/dt limitation by influencing both L and v_c. Small values of O (i.e. large values of L and C), mean smaller values of di/dt from equation (14) and (15); and relative smaller switching losses. As a result, the value of O will be a trade-off between switching losses and distortion of the current waveform.

The distortion in the current waveform arising in Mode 2, however, can be reduced by increasing the value of v_c, i.e. the parameter ν, equation (10). When the active filter is required to generate a harmonic of order h, the capacitor voltage v_c has oscillations of (h±1)f and 2hf frequencies. This limits the maximum value of I_h/I that will still allow the equation (16) to be satisfied.

In the inductive mode of equation, the current through the convertor cannot exceed the limit $I_{pn} = \frac{I}{V/(L\omega)} = \frac{I}{I_{nat}}$, where I_{nat} is the line current that is obtained when the converter bridge is shorted. In the capacitive mode, this restriction does not apply. As the current is increased, the distortion will also increase because the (h±1)f and 2h frequency oscillations in v_c will increase. Thus, increasing I_{nat} will increase the distortion in the converter current waveform.

The effect of all above parameters is to cause deviation of the current that is generated by the active filter from the desired waveform, and the actual line current has a form different of the (7):

$$i = \sqrt{2} I_1' \sin(\omega t \pm 90^\circ) + \sum \sqrt{2} I_{hm} \sin(mh\omega t + \theta_{hm}) \qquad (17)$$

In the below simulations based on the mathematical model described above, and realized with some programs in C++ and Matlab, the active filter limitations at the desired harmonic frequency hf, were quantified with the help of two measures:

$$\text{percentage magnitude error} = [(I_h - I_{hh})*100]/I_h \qquad (18)$$
$$\text{phase error} = \theta_h - \theta_{hh} \qquad (19)$$

The two measures from equations (18) and (19), i.e. active filter limitations, are computed for I_h/I as long as condition given in (16) is satisfied, and are plotted versus I_h/I.

5.2 Comments based on the magnitude and phase error plot.

Some of the magnitude and phase graphs, presented in Fig. 5 a,b through Fig. 16 a,b, quantify the limitations of the active filter operation. The magnitude and phase error plots are obtained for different orders of h (=3,5,7,9), in the capacitive and inductive modes, two different values of I_{pu} (= 0.1 and 0.05), four different values of θ_h (= -90°, 0°, 90°, 180°), different values for ν and Ω.

From all these plots the following conclusions were observed, and extracted:

Capacitive mode of operation (Fig. 5 a,b – Fig. 10 a,b):

- the magnitude and phase errors are higher for higher values of I_{pu}, and also for higher values of I_h/I;
- the magnitude error and the phase error are high for θ_h = -90°and 0°, and low for θ_h = 180° and 90°;
- the lowering of Ω have as result a considerable increase in both the measures;
- an increase in the order of h (3,5,7,9 …) also increases the deviation of the actual current from the desired current waveform;

Inductive mode of operation (Fig. 11 a,b – Fig. 16 a,b):

- the comparison for the some order of h between the inductive mode of operation and the capacitive mode for I_{pu} = 0.1, ν = 1.2 and Ω = 1.5 (the values from plots), indicates that the magnitude and phase errors due to the deviations of the active filter current from the desired waveform are very comparable. The conclusion is that the same effects of the four parameters are and in the inductive mode of operation.

Fig 5.a Mag. errors; cap. mode, h=3, Ipu=0.1

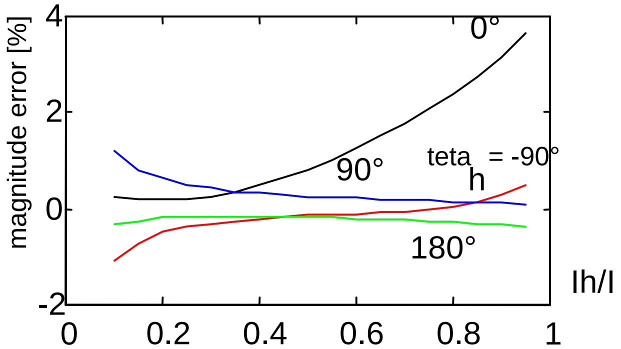


Fig 5.b Phase Errors; cap. mode, h=3, Ipu=0.1

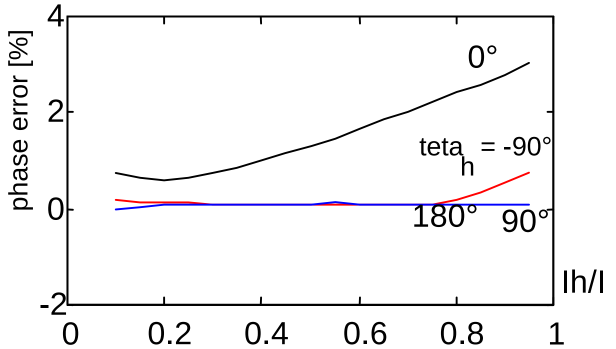


Fig 6.a Mag. errors; cap. mode, h=5, Ipu=0.1

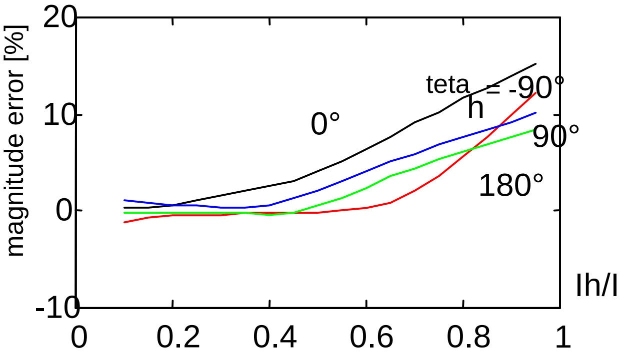


Fig 6.b Phase Errors; cap. mode, h=5, Ipu=0.1

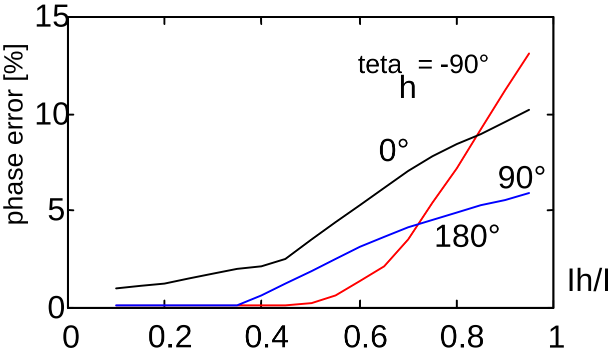


Fig 7.a Mag. errors; cap. mode, h=7, Ipu=0.1

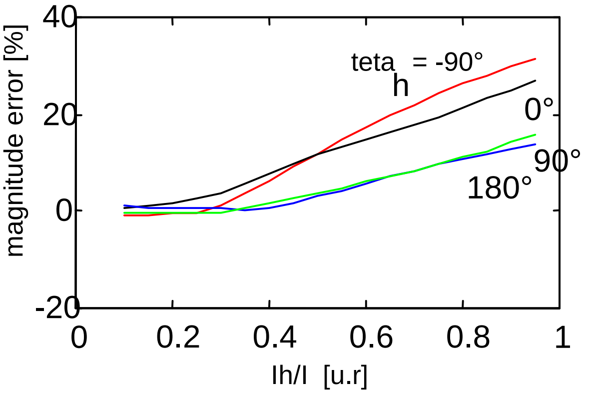


Fig 7.b Phase Errors; cap. mode, h=3, Ipu=0.1

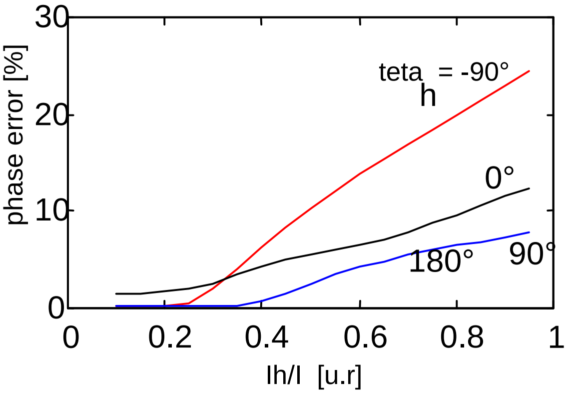


Fig 8.a Mag. errors; cap. mode, h=3, Ipu=0.05

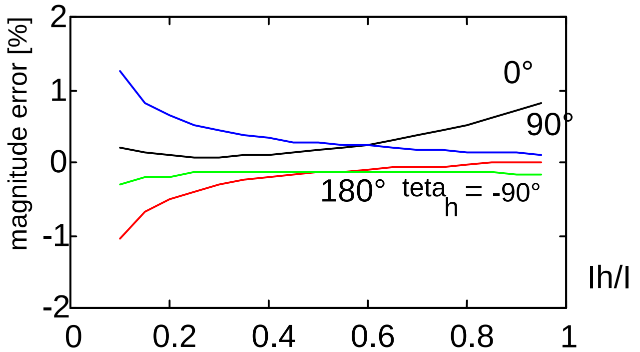


Fig 8.b Phase Errors; cap. mode, h=3, Ipu=0.05

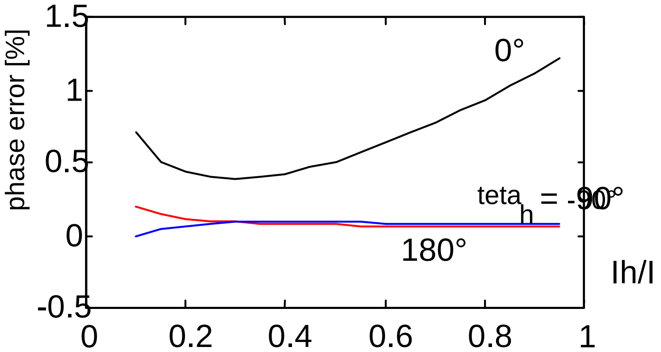


Fig 9.a Mag. errors; cap. mode, h=5, Ipu=0.05

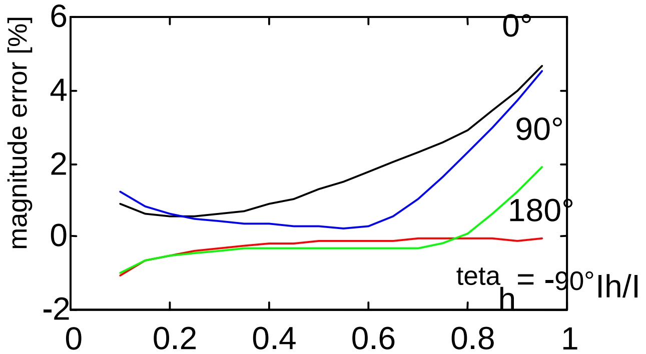


Fig 9.b Phase Errors; cap. mode, h=5, Ipu=0.05

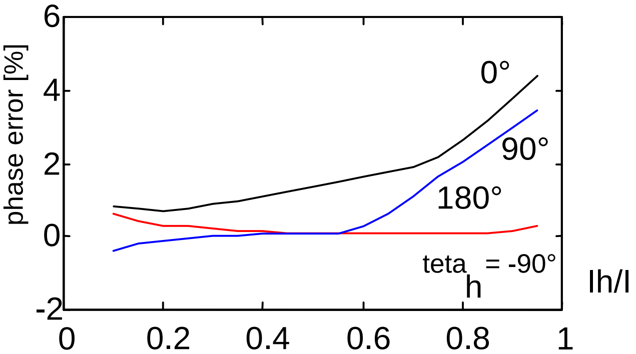


Fig 10.a Mag. errors; cap. mode, h=7, Ipu=0.05

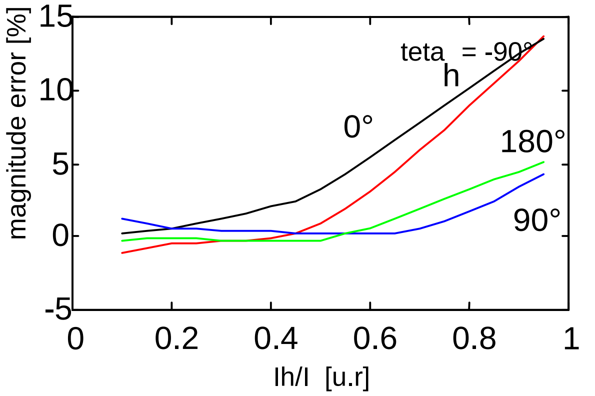


Fig 10.b Phase Errors; cap. mode, h=3, Ipu=0.05

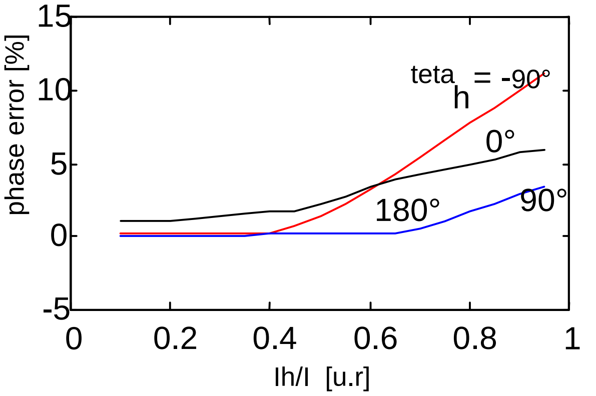


Fig 11.a Mag. errors; ind. mode, h=3, Ipu=0.1

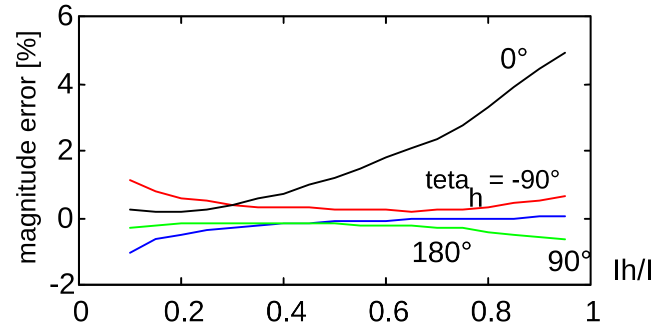


Fig 11.b Phase errors; ind. mode, h=3, Ipu=0.1

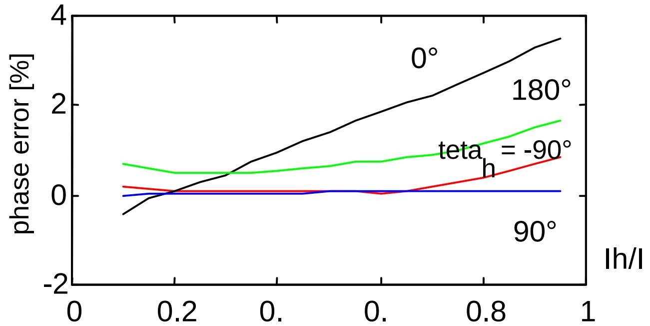


Fig 12.a Mag. errors; ind. mode, h=5, Ipu=0.1

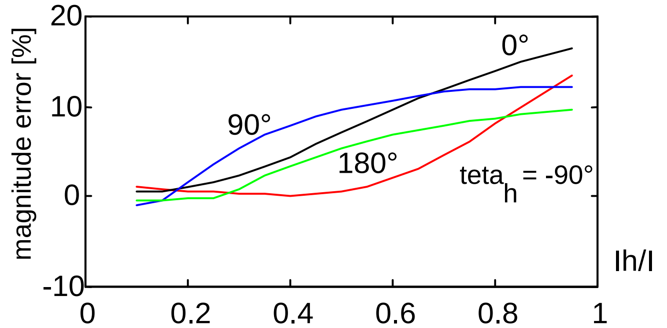


Fig 12.b Phase errors; ind. mode, h=5, Ipu=0.1

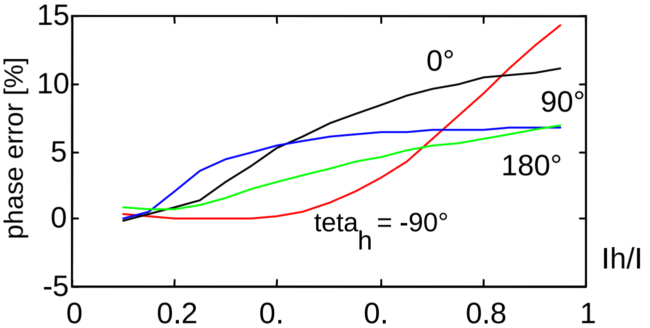


Fig 13.a Mag. errors; ind. mode, h=7, Ipu=0.1

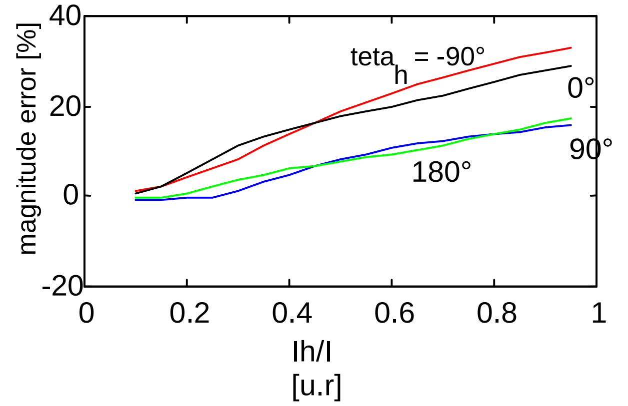


Fig 13.b Phase errors; ind. mode, h=3, Ipu=0.1

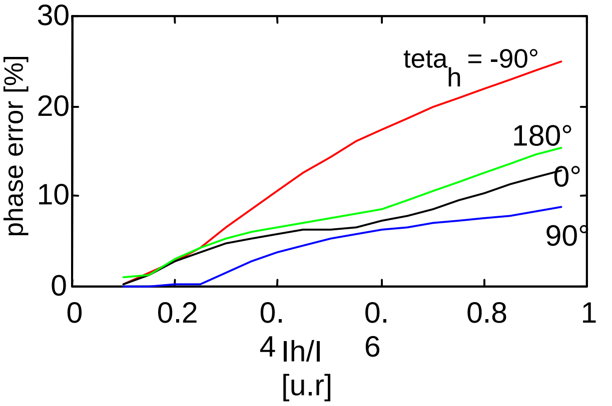


Fig 14.a Mag. errors; ind. mode, h=3, Ipu=0.05

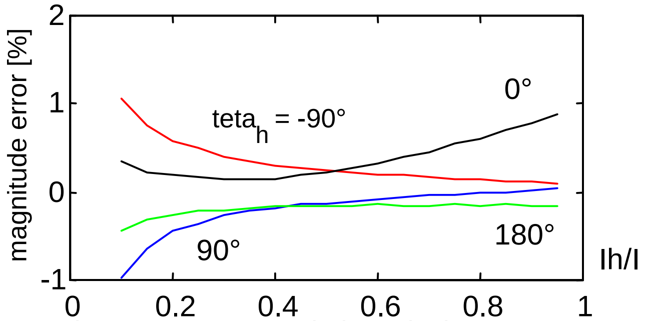


Fig 14.b Phase errors; ind. mode, h=3, Ipu=0.05

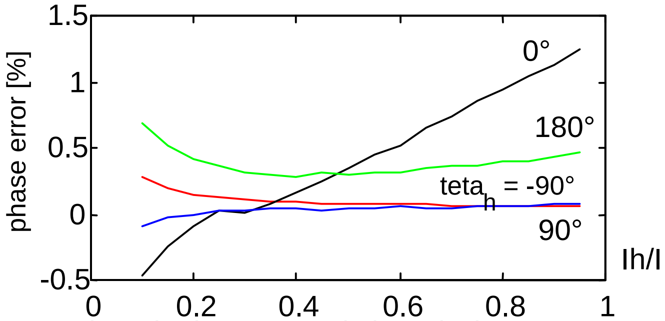


Fig 15.a Mag. errors; ind. mode, h=5, Ipu=0.05

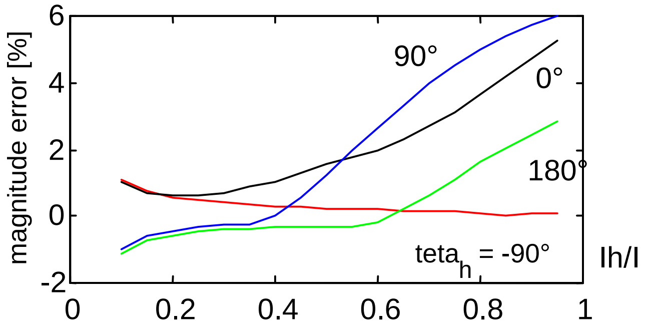


Fig 15.b Phase errors; ind. mode, h=5, Ipu=0.05

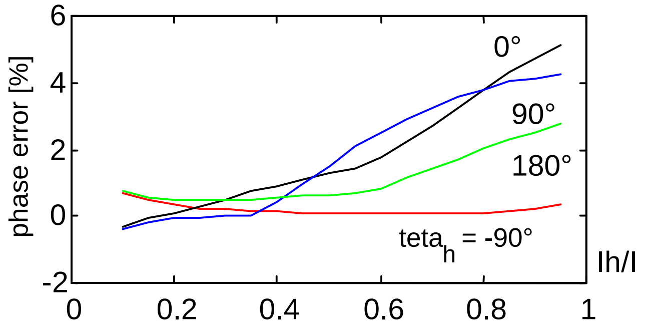


Fig 16.a Mag. errors; ind. mode, h=7, Ipu=0.05

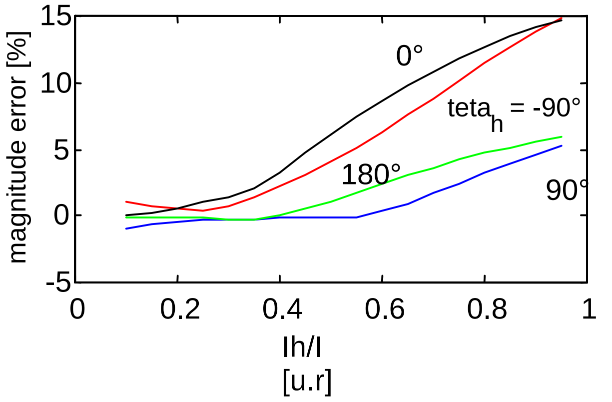
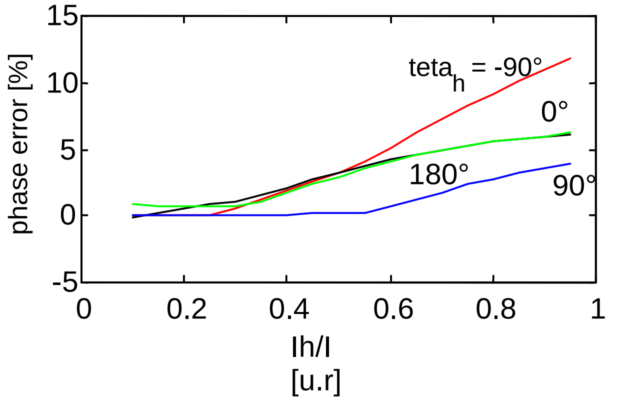


Fig 16.b Phase errors; ind. mode, h=3, Ipu=0.05



6. CONCLUSIONS

For a circuit consists of an inductance in series with a switched capacitor network, able to operate as a 50 Hz reactive power (lead or lag) compensator, as an active power line conditioner, and as an active filter, little studied in literature, were investigated the limitations and constraints, in the operation mode as an active filter.

To analyze these limitations, an analytical approach based on simulation of the circuit transients using difference equations, was used. The main limitation of the active filter, which arises from its inability to produce current waveforms with the desired di/dt, was quantified by the agency of the percentage harmonic magnitude error and harmonic phase error.

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