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PLL MODEL FOR GRID VOLTAGE REFERENCE RECONSTRUCTION

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Abstract: In power electronics area, the PLL (Phase Lock Loop) circuit is needed to reconstruct the sinusoidal reference signal used on the APF (active power filters) or grid-tied inverters, starting from the distorted grid voltage. Research area of the APF focuses more on the current of voltage control loops and less on the sinusoidal reference signal, usually considered available by default. Implementing in practice such a circuit poses difficulties since the available PLL integrated circuits are designed for digital telecommunication area, where signals are digital and a small phase error is acceptable. This paper presents a phase lock loop model with harmonic output and zero phase error during normal use.

Keywords: PLL, sinusoidal output, grid synchronization, distorted input signal

INTRODUCTION

Operating with clean, synchronized, sinusoidal currents and voltages represents the ideal situation for the energy generation and transportation system. Almost all the nonlinear low-power devices uses the same principle for energy conversion (grid - transformer - uncontrolled rectifier - capacitive-resistive load) and the created distortions are summing up in the main grid. The effect observed by the customers is the distorted grid voltage; the effects observed by the energy distribution system consist in increasing losses and saturation of the transformers.

Active power filters are wide used to compensate the over polluted grids. An APF uses power electronics to control the electrical current that flows from the grid to the customers. Some control loops in the APF computes the instantaneous current that must be injected in the grid to compensate for the load's current harmonics or reactive power. Zero reactive power implies that the current and voltage signals are always perfectly synchronized. If the APF uses a reference signal non-harmonic, the regulated current will reproduce those distortions too; if the APF uses a reference with phase delay, it will create reactive power in the system.

Practical implementation of such a circuit implies the use of a PLL circuit to reconstruct the harmonic reference. Most of the integrated circuits available on the market are designed for the digital signal processing, thus the output signal is rectangular (and useless for the APF). Most modern signal synthesizer circuits are digital and allows for synchronization of the output signal (harmonic too) with an external signal, if they are properly configured by an external processor. The complexity of the resulted schematic is considered usually not to worth and the distorted grid voltage is used as reference instead.

The presented paper offers a methodology and a mathematic model that can be used to design a PLL circuit with sinusoidal output, with negligible phase error between input and output signal.

BACKGROUND

1.1. The PLL block diagram

The Fig. 1 block schematic represents the structure of the generic PLL circuit. The signals $v_i(t)$, v_d(t), $v_v(t)$ and $v_r(t)$ are high speed variation signals compared with the slow varying signal $v_c(t)$.

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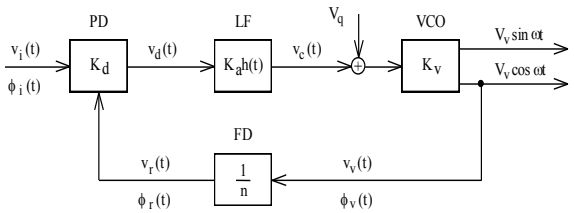

Fig.1. The PLL circuit block diagram

The PLL circuits must be customized according to each application:

- **PD = Phase Detector.** This block is a multiplier or a sequential digital circuit that gives the phase error signal $v_d(t)$. In our application the phase detector circuit is a Gilbert cell value to value multiplier where the input signal $v_i(t)$ is the line voltage, and $v_r(t)$ the quadrature VCO cosine output signal (see 3.1 section). The PD operation is described by equation:

$$(1)\ v_d(t) = K_d \sin\left(\varphi_i(t) - \varphi_r(t)\right) \quad .$$

- **LF = Loop Filter.** The block consists of a filter, and optional an amplifier. The time domain loop filter dynamic model is:

$$(2)\ v_c(t) = K_a\ h(t) * v_d(t) \quad .$$

- **VCO = Voltage Controlled Oscillator.** Usual is a relaxation oscillator that generates a square wave signal. In this application a quadrature oscillator is used, with two output signals: the sine signal is used as the actual and the cosine signal is the PLL feedback signal. The VCO instantaneous frequency is

$$(3)\ \omega_v(t) = K_v\left(v_c(t) + V_q\right) \quad .$$

  When input signal is missing or when there are a significant difference between $v_i(t)$ and $v_r(t)$ frequencies, the PLL circuit quiescent frequency is $\omega_q = K_v V_q$.

- **FD = Frequency Divider.** The DF block is used when output signal frequency must be N times greater than the input frequency. Is no need of frequency divider in our application.

1.2. The dynamic model of the PLL loop

Applying the Laplace transform to the Fig.1 schematic, results the dynamic model presented in Fig.2.

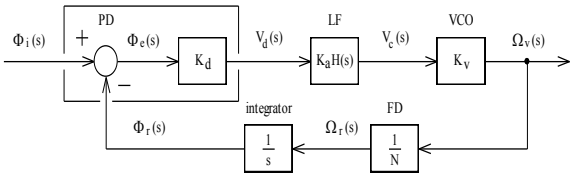

Fig.2. The PLL dynamic model

After the linearization of the (1) equation, the phase detector block is represented as a phase subtraction block and a constant multiplier. The linear PLL blocks equations are:

$$(4)\ \Phi_e(s) = \Phi_i(s) - \Phi_r(s)$$

$$(5)\ V_d(s) = K_d\,\Phi_e(s);\ \dim\left[K_d\right] = \frac{V}{rad}$$

$$(6)\ V_c(s) = K_a\,H(s) V_d(s);\ \dim\left[K_a\right] = 1$$

$$(7)\ \Omega_v(s) = K_v\,V_c(s);\ \dim\left[K_v\right] = \frac{rad}{V\,s}$$

$$(8)\ \Omega_r(s) = \frac{\Omega_v(s)}{N};\ \dim\left[N\right] = 1$$

$$(9)\ \Phi_r(s) = \frac{1}{s}\,\Omega_r(s);\ \dim\left[\frac{1}{s}\right] = s$$

In Fig.2, $V_d(s)$ and $V_c(s)$ are Laplace images of $v_d(t)$ and $v_c(t)$ signals. The quantities $\varphi_i(t)$, $\varphi_e(t)$, $\omega_v(t)$, $\omega_r(t)$, and $\varphi_r(t)$ there are no signals, but being time-varying physical quantities, they have the Laplace transforms: $\Phi_i(s)$, $\Phi_e(s)$, $\Omega_v(s)$, $\Omega_r(s)$, $\Phi_r(s)$.

Eliminating the intermediate variables $V_d(s)$, $V_c(s)$, $\Omega_v(s)$, and $\Omega_r(s)$, from the previous set of equations we get the open-loop transfer function:

$$(10)\ H_{OL}(s) = \frac{K_d\,K_a\,K_v}{N\,s} H(s)$$

In control engineering the linear feedback loop consist in two entities: the plant (all the engines, mechanisms, transducers, actuators that perform the fabrication process) and the automate controller.

The PLL circuit plant parts are: PD, VCO and FD blocks, which lead to the integrator behaviour of the plant transfer function:

$$(11)\ H_{Plant}(s) = \frac{K_d\,K_v}{N\,s} = \frac{1}{s\,T_1}$$

Given the fact that K_d, K_v and N are fixed values, we denote $T_1 = N/(K_d\,K_v)$ as the integrator's time constant.

Also the LF block, described by equation (6) is the PLL circuit automate controller. Changing the LF structure and parameters we change the behaviour and the performance of PLL circuit.

1.3. PLL circuit types

According to the number of integrators in the open loop transfer function, the PLL circuits are of two classes:

- Ttype-1 PLL circuit has a single integrator in plant transfer function (11). In that case the loop filter is a linear LPF filter. The type-1 PLL has no steady-state frequency error but has steady-state phase error
- Type-2 has two integrators in open-loop transfer function one in the plant transfer function and the other in the LF block. The type-2 PLL circuit has no steady-state errors.

In our proposed solution, the loop filter will commute from type-1 to type-2 PLL at the proper moment. The two loops will be designed independently, to obtain the best performances for both situations.

MOTIVATION

Our goal is to find a PLL circuit design method that gives an output frequency reference synchronous with line voltage fundamental and that have no phase errors. The solution is a type-2 PLL circuit with multiplying phase detector.

1.4. Filtering effect of the value to value multiplying phase detector

The feedback signal is the quadrature VCO cosine output signal that have no distortions:

$$(12)\quad v_r(t) = A_r \cos(\omega t + \varphi_r) \quad .$$

In the Fig.1 circuit, the input signal is the line voltage. In practice, $v_i(t)$ is a slowly varying 50 Hz alternative signal with 3…5 % harmonic distortions. The $v_i(t)$ fundamental component is:

$$(13)\quad \begin{aligned} v_1(t) &= A_1 \sin(\omega t + \varphi_1) \\ &= A_1 \left(\sin \omega t \cos \varphi_1 + \cos \omega t \sin \varphi_1\right) \end{aligned}$$

where we can highlight the Fourier coefficients:

$$(14)\quad \begin{aligned} v_1(t) &= a_1 \cos \omega t + b_1 \sin \omega t \\ a_1 &= A_1 \sin \varphi_1 \quad ; \quad b_1 = A_1 \cos \varphi_1 \end{aligned}$$

Given the fact that the input signal is a periodic one, it can be decomposed in the Fourier series:

$$(15)\quad v_i(t) = \frac{1}{2} a_0 + \sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{n=1}^{\infty} b_n \sin n\omega t$$

Because the line voltage has no continuous component, it is obvious that $a_0 = 0$.

The Gilbert cell multiplier operation is given by the equation:

$$(16)\quad v_d(t) = \frac{v_i(t) v_r(t)}{k} \quad , \quad \text{where } \dim[k] = V \, .$$

Multiplying $v_i(t)$ and $v_r(t)$ results:

$$(17)\quad v_d(t) = \frac{A_r}{k} \left(v_1(t)\right) \cos\left(\omega t + \varphi_r\right)$$

If $v_i(t)$ and $v_r(t)$ are the same frequency stationary signals, it is sufficient to study a single period of the $v_d(t)$ signal to know the signal behaviour. If the loop filter eliminates all the $v_d(t)$ alternative components the continuous components are:

$$(18)\quad \overline{v_d(t)} = \frac{A_r}{k} \int_{t=t_0}^{t_0+T} \left(\sum_{n=1}^{\infty} a_n \cos n\omega t + \sum_{n=1}^{\infty} b_n \sin n\omega t \right) \cos(\omega t + \varphi_r)\, dt$$

All the terms calculated for n ≠ 1 are alternative components and will be removed by the loop filter, so that the filtered $v_d(t)$ signal remains:

$$(19)\quad \begin{aligned} \overline{v_d(t)} &= \frac{A_r}{k} \left(\frac{a_1}{2} \cos(-\varphi_r) + \frac{b_1}{2} \sin(-\varphi_r) \right) \\ &= \frac{A_r}{2k} \left(a_1 \cos \varphi_r - b_1 \sin \varphi_r \right) \end{aligned}$$

Substituting a_1 and b_1 coefficients from (14) we get:

$$(20)\quad \begin{aligned} \overline{v_d(t)} &= \frac{A_r}{2k} \left(A_1 \sin \varphi_1 \cos \varphi_r - A_1 \cos \varphi_1 \sin \varphi_r \right) \\ &= \frac{A_1 A_r}{2k} \sin(\varphi_1 - \varphi_r) \end{aligned}$$

In (20) we denote $K_d = (A_1 A_r)/2k$. For small phase difference, the equation (20) can be linearized as:

$$(21)\quad v_c(t) \approx \overline{v_d(t)} = K_d \cdot \left(\varphi_1 - \varphi_r\right)$$

Conclusion: for the input signal $v_i(t)$, only the phase of the fundamental component is present in equation (20), which means that the value to value multiplier eliminates all the harmonic content of the input signal, but only if the feedback signal is a pure cosine shape signal.

1.5. The commutable loop filter

It is well known that type-2 PLL circuit must use a phase-and-frequency detector (PFD) that guarantees the success of capture process. The PFD circuit acts in two steps: first control the VCO frequency near to the input signal frequency, then syncs the VCO signal phase to the input signal phase.

The PFD circuit is a sequential digital circuit with input signal and the feedback signal is digital. The Fig. 3 Matlab simulation shoes that the zero crossing detector usage to transform the distorted line voltage in a digital signal produces phase errors.

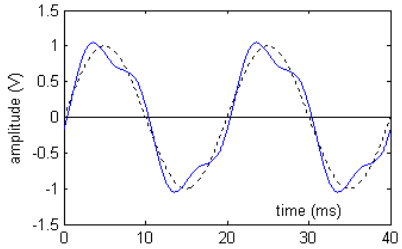

Fig.3. The zero crossing phase detector errors

In our project we use two loop filters:

- A 1st order LPF filter used to synchronise the VCO frequency with the line frequency.
- An integrator and a lead-lag filter used for PLL loop normal operation.

The switching command is given after an estimated time required for synchronization circuit. So the capture problem is solved by switching the loop filter.

TYPE-1 PLL CIRCUIT DESIGN METHOD

The loop filter design is pursuing two objectives: to best attenuate the $2f_q$ frequency, and to ensure that the capture band is wide enough.

1.6. The module criterion

The module criterion requires that open-loop transfer function of dynamic system must be approximated by a transfer function such that:

$$(22)\quad H_{OL}(s) \cong \frac{1}{2T_\Sigma\, s\,(sT_\Sigma + 1)}$$

If the approximation (22) is valid, the closed-loop transfer function will be a 2nd order low-pass Butterworth filter, with flat magnitude-frequency characteristic and aperiodic response at step signal.

For the PLL circuit start-up sequence we propose the simplest 1st order low pass filter as loop filter.

$$(23)\quad H_{LF}(s) = \frac{K_a}{sT_2 + 1}$$

With $H_{Plant}(s)$ from (11) and $H_{LF}(s)$ from (23) we get the PLL circuit open loop transfer function:

$$(24)\quad H_{OL}(s) = \frac{1}{sT_1} \cdot \frac{K_a}{sT_2 + 1}$$

Identifying (22) and (24), results:

$$(25)\quad \frac{1}{sT_1} \cdot \frac{K_a}{sT_2 + 1} \equiv \frac{1}{2sT_\Sigma\,(sT_\Sigma + 1)}, \quad T_2 = T_\Sigma;\quad K_a = \frac{T_1}{2T_\Sigma}$$

From the module criterion results also the link between the dimensionless constant K_a and time constants T_1 and T_Σ. In (35) T_Σ represents the LPF time constant and f_Σ is the corner LPF frequency:

$$(26)\quad f_\Sigma = \frac{1}{2\pi T_\Sigma},$$

1.7. Maximum tracking bandwidth

The design method of the "type-1" PLL circuit is complete with an estimation model for the tracking mode bandwidth.

Let us consider a specified PLL circuit with A_i, A_r, k, K_d and K_v parameters of known values. The estimation of the maximum frequency deviation is computed starting from the of the value to value multiplying phase detectors output signal:

$$(27)\quad v_d(t) = \frac{A_i A_r}{2k}\sin\left(\varphi_i(t) - \varphi_r(t)\right)\ .$$

Because of max[sin(•)] = 1, from nonlinear equation (27) results the maximum $v_d(t)$ value is

$$(28)\quad \max\left[v_d(t)\right] = \frac{A_i A_r}{2k}$$

We denote Δf_{max} the maximum frequency deviation that the PLL circuit can track. If we suppose that the loop filter eliminates completely the $2f_q$-frequency component, from (28) results:

$$(29)\quad \Delta f_{\max} = \frac{A_i A_r}{2k} K_a K_v$$

The Δf_{max} represents the theoretical limit for both the capture bandwidth and the tracking bandwidth.

1.8. Gain influence on step signal response

The evaluation of the K_a factor must be carried only after the K_d, K_v, T_1 and T_Σ have been determined, so that all parameter evaluation errors and arithmetic errors to accumulate in the value of K_a.

The Fig.4 plots are a study for K_a parameter influence on the 2nd order dynamic system step response.

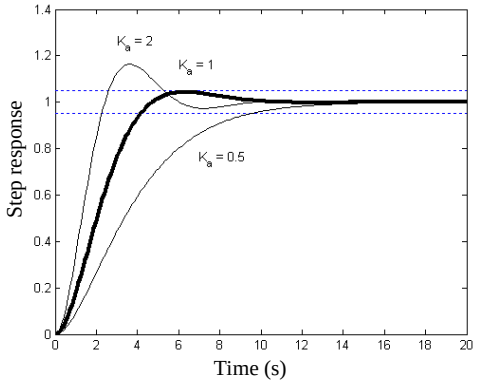

Fig.4. K_a influence on the 2nd order dynamic system step response

Results are obtained Matlab using feedback and step functions. The analysis of the closed-loop system, was done starting to the open-loop transfer function:

$$(30)\quad H_{OL}(s)=\frac{B(s)}{A(s)}=\frac{K_a}{2T_\Sigma\, s(sT_\Sigma+1)}$$

The step response was recorded for 20 seconds, considering T_Σ = 1 second. It can be observed that:

- for K_a > 1, the step signal response is oscillating;
- for K_a < 1, the step signal response is slower than the aperiodic response.

So**,** the optimum theoretical value of K_a is 1, value for which the stabilisation time is minim, the response at step input signal is aperiodic (overshoot without oscillations) and the frequency response is of maximum flat shape.

Because of K_a evaluation errors, an adjustable gain circuit is needed to experimentally adjust the optimum response $v_c(t)$ of the PLL circuit at frequency step input.

1.9. A type-1, 50Hz PLL design example

On a 50 Hz PLL circuit, with 1st order loop filter, with no frequency divider (N = 1), the VCO constant is K_v = 50 Hz/Vs and the value to value multiplying phase detector parameters are $A_1 = A_r = k = 1$ V.

First, we must evaluate the plant parameters. From equation (20), results the phase detector constant:

$$(31)\quad K_d=\frac{A_1 A_r}{2k}=0.5\,\frac{\mathrm{V}}{\mathrm{rad}}$$

We observe that in enounce K_v constant is in Hz/V, in so (11) we substitute $2\pi K_v$ and we calculate the plant model time constant T_1:

$$(32)\quad T_1=\frac{N}{K_d\,K_v}=\frac{1}{0.5\dfrac{\mathrm{V}}{\mathrm{rad}}\times 2\pi\times 50\dfrac{\mathrm{rad}}{\mathrm{Vs}}}=\frac{1}{50\pi}\ \mathrm{s}$$

Second, we must calculate the necessary loop filter parameters f_Σ and K_a knowing that the PLL circuit quiescent frequency f_q is 50 Hz.

Let us denote $0 < a_r < 1$ the 1st order LPF attenuation expressed as a ratio, and $a_{dB} = 20 \lg a_r$ is the same attenuation in dB. The loop filter design starts with the choice of the LPF attenuation at $2f_q$ frequency. Consequently, the 1st order LPF filter corner frequency expressed by a_r attenuation is:

$$(33)\quad f_\Sigma=2\,f_q\,a_r=2\times 50\mathrm{Hz}\times a_r=100\times a_r\ \mathrm{Hz}$$

Because $T_\Sigma = 1/2\pi f_\Sigma$ and using (25) equation we get:

$$(34)\quad K_a=\frac{T_1}{2T_\Sigma}=\frac{T_1}{2}\,2\pi\,f_\Sigma=T_1\,\pi 2\,f_q\,a_r$$

Because $T_\Sigma = 1/2\pi f_\Sigma$ and using T_1 the plant parameter value from (25), we calculate the adimensional K_a constant expression

$$(35)\quad K_a=\frac{\mathrm{s}}{50\pi}\,\pi 2\times 50\,\mathrm{s}^{-1}a_r=2\,a_r$$

Also equation (29) can be customised. We express Δf_{max} by attenuation:

$$(36)\quad \Delta f_{\max}=0.5\,\mathrm{V}\times 2\,a_r\times 50\frac{\mathrm{H_z}}{\mathrm{V}}=50\times a_r\ \mathrm{H_z}$$

Equations (33), (35) and (36) were used to compute the table 1 circuit parameters calculated for three situation a_{dB} = -20, -30 and -40 dB.

a_{dB}	a_r	f_Σ (Hz)	K_a	Δf_{max} (Hz)
-20	0.1	10	0.200	5.00
-30	0.0316	3.16	0.062	1.58
-40	0.01	1.0	0.020	0.50

Table 1. The Type-1 PLL trade-off table

The 2nd column is a_r, attenuation as a ratio, the 3rd column is f_Σ, the LPF filter corner frequency, the 4th column is the K_a constant, and the 5th column is Δf_{max}, the maximum frequency deviation that a specified PLL circuit can do.

The decision making is a trade-off subject with two quality criteria:

- The a_{dB} growing, is an improvement because of $2f_q$ frequency component modulate in frequency the VCO output signal;

- A good attenuation means that a_r decreases and the Δf_{max} decreases too (see (36) eq.). So the capture bandwidth reduces.

TYPE-2 PLL CIRCUIT DESIGN METHOD

Similar chapter 4, we developed a design method that the loop filter of the type-2 PLL circuit can be tuned starting from the attenuation of the $2f_q$ component.

1.10. The symmetry criterion

The control engineering design method used to tune the type-2 loop filter is symmetry criterion. The criterion requires that the dynamic system open-loop transfer function to can be approximated by:

$$(37)\quad H_{OL}(s)=\frac{4T_\Sigma s+1}{8T_\Sigma^2 s^2(T_\Sigma s+1)}$$

Since plant the transfer function (11) is an integrator, from (37) results that the Loop filter must be composed from an integrator and a lead-lag filter:

$$(38)\quad H_{LF2}(s)=\frac{K_a}{T_{\text{int}}\,s}\cdot\frac{T_z s+1}{T_p s+1}$$

From (11) and (38) results that the type-2 PLL circuit open-loop transfer function is:

$$(39)\quad H_{OL}(s)=\frac{1}{T_1 s}\cdot\frac{K_a}{T_{\text{int}}\,s}\cdot\frac{T_z s+1}{T_p s+1}$$

The transfer function (33) was factorised in three distinct parts: the plant model where $T_1 = N/(K_dK_v)$, the loop filter integrator and the lead-lag filter. Identifying the (37) and (39) on obtain:

$$(40)\quad \frac{1}{T_1 s}\cdot\frac{K_a}{T_{\text{int}}\,s}\cdot\frac{T_z s+1}{T_p s+1}\equiv\frac{4T_\Sigma s+1}{8T_\Sigma^2 s^2(T_\Sigma s+1)}$$

The K_a parameter and the lead-lag parameters T_z and T_p results from next equations:

$$(41)\quad \frac{K_a}{T_1}\cdot\frac{1}{T_{\text{int}}}=\frac{1}{8T_\Sigma^2}\quad\Rightarrow\quad K_a=\frac{T_1 T_{\text{int}}}{8T_\Sigma^2}$$

$$(42)\quad \frac{T_z s+1}{T_p s+1}=\frac{4T_\Sigma s+1}{T_\Sigma s+1}\quad\Rightarrow\quad\begin{cases}T_z=4T_\Sigma\\ T_p=T_\Sigma\end{cases}$$

If the T_Σ value is chosen first, the (41) equation is a link equation between T_{int} and K_a parameters.

1.11. Gain influence on the phase margin

Similar as discussed in section 4.3, all the parameter evaluation errors and arithmetic errors accumulates in K_a parameter value.

In Fig. 5 is a Matlab simulation for gain influence on phase margin. The Bode diagrams were plotted for a system with parameters: f_{cut}=1 Hz, f_p=2 Hz, f_z=0.5 Hz. The time constants results from (41) equations: $T_p=T_\Sigma$, $T_z=4T_\Sigma$ and $T_\Sigma=2/(2\pi f_{cut})$.

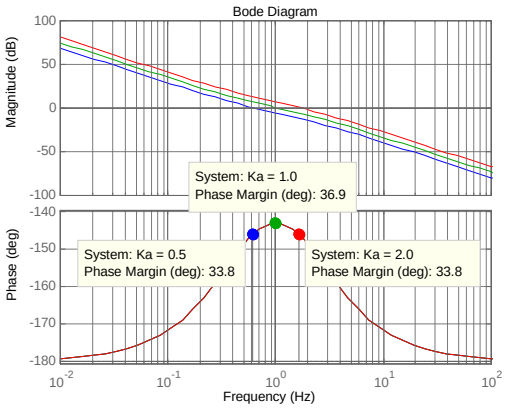

Fig.5. Bode diagram for the open-loop circuit

The simulation were done for three values of K_a parameter. In Fig. 5 we observe that any gain error reduces the PLL circuit phase margin.

The open-loop transfer function (39) presents two poles in the origin, that means a 180° phase delay at low frequencies. The zero ($4T_\Sigma s+1$) presence at one octave under the cut frequency introduces a phase margin of 36.9° but with the cost of 43% overshoot.

1.12. Commutable loop filter implementation

It is known that the integrator circuit cannot operate in open loop configuration. So the Fig.6 schematic is our solution for type-2 loop filter integrator:

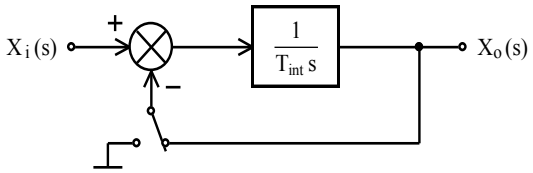

Fig.6. Stand-by loop filter integrator

If the switch is connected to the ground, the circuit is an integrator with time constant T_{int}, and if the switch closes the negative feedback loop then the circuit is a LPF filter:

$$X_o(s)=\frac{1}{T_{\text{int}}s}\left(X_i(s)-X_o(s)\right)$$

$$(43)\quad \frac{X_o(s)}{X_i(s)}=\frac{1}{T_{\text{int}}s+1}$$

The Fig. 7 block diagram is the complete PLL circuit loop filter. The two switches are in start-up position. After a time interval required for synchronization, the switching command connects simultaneous the inte-

grator and lead-lag filter in signal path and then the type-2 PLL circuit begin to operate.

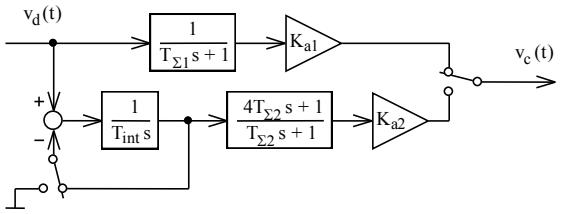

Fig.7. The loop filter block diagram

In stand-by operation mode type-2 loop filter path have the transfer function:

$$(44)\quad \frac{V_c(s)}{V_d(s)} = \frac{1}{T_{int}s+1}\cdot\frac{T_z s+1}{T_p s+1}\cdot K_{a2}$$

The K_{a1} and K_{a2} parameters in Fig.6 must be computed such that in the switching moment the two signal paths to have equal continuous components. So the (23) transfer function DC gain to match the (44) transfer function DC gain:

$$(45)\quad \lim_{s\to 0}\frac{K_{a1}}{T_2 s+1} = \lim_{s\to 0}\frac{K_{a2}}{T_{int}s+1}\cdot\frac{T_z s+1}{T_p s+1}$$

Results that $K_{a1} = K_{a2}$. This will guarantee no step variation of the VCO input signal in the commutation moment.

1.13. Simulation results

The presented model was implemented in Matlab/Simulink simulation module:

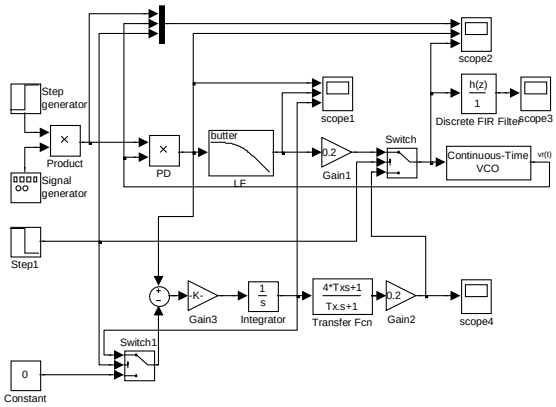

Fig.8. The simulation model

As already stated, the integrator is kept in reset state until the type-1 PLL synchronizes and only then it is activated.

Fig. 9 presents the following signals: channel 1: green: cosine signal from the VCO, blue – PLL's input signal, red – command to activate the integrator (active on low state); channel 2: phase detector's output signal, channel 3: control signal for the VCO.

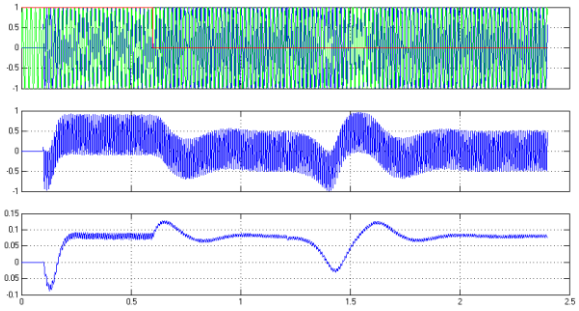

Fig.9. The simulation results

It can be observed that the output of the phase detector is an oscillating signal (with double the input frequency), who's mean value is proportional with the phase difference. After filtering, the signal applied to the VCO assures proper operation of the control loop.

At time *t=1.25s*, after the type-2 PLL structure has settled, a strong perturbation is introduced on the input signal (180 phase degree change). This perturbation is higher than any real phase perturbation could affect the grid voltage, but the control loop does not loose its synchronization.

In Fig.10, the input (red) and output (blue) signals are detailed, and it can be clearly seen that the harmonic content of the input signal does not perturb the operation of the proposed control loop.

The input signal contain 3th and 5th harmonics, each with 10% amplitude relative to the fundamental component:

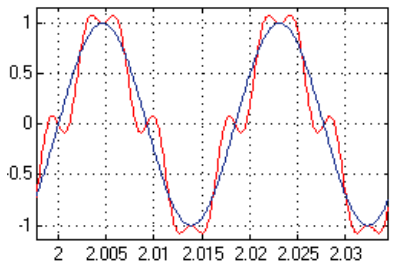

Fig.10. Detail of the synchronised input and output

CONCLUSIONS

This paper presented a variable structure PLL circuit that can be used to reconstruct the sinusoidal reference, essential for correct operation of many grid-connected electronic devices (active power filters, inverters etc.).

The proposed structure is based on a combination of three key elements:

- the value-to-value multiplier phase detector, that compare the phases of the input and feedback signals all the time of the period,
- the quadrature harmonic voltage controlled oscillator that outputs both sine and cosine signals – from which the cosine is used by the PLL feedback loop and the sine is the output desired signal,
- the variable structure of the loop filter, that switches from a low-pass first order filter after the lock sequence has completed to a integrator followed by a lead-lag filter to assure zero stationary error between input and output signals.

The proposed circuit switches from a "type-1" to a "type-2" PLL circuit at the proper moment of time. The design steps for "type-1" circuit are presented and are based on the use of the module criterion to analyze the open-loop transfer function of the circuit. This criterion guarantees the best closed-loop behavior. The design method for "type-2" PLL circuit is based on the symmetry criterion. Even if the "type-2" PLL have unwanted oscillatory response to the step input signals, the complete structure of the presented circuit guarantee that no step variation is applied for the "type-2" PLL structure.

The switching command is given after an estimated time required for synchronization circuit.

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